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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10832	(processor near4 synchroniz\$5)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2006/10/25 15:14
L2	31	(processor near4 synchroniz\$5) and (tick near4 counter)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2006/10/25 15:19
L3	9	(tick near4 counter).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2006/10/25 15:20
L4	41	(tick near4 counter).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2006/10/25 15:59
L5	18	(tick near4 counter).clm. and synchroniz\$5	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2006/10/25 15:59
S1	1	("6199169").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/10/25 15:14
S2	1	("6449290").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/07/22 18:05
S3	162	tick adj2 counter	US-PGPUB; USPAT	OR	ON	2004/07/22 18:05
S4	45	(tick adj2 counter) and synchroniz\$6 and off\$set	US-PGPUB; USPAT	OR	ON	2004/07/22 18:21
S5	71	(tick adj2 counter) and synchroniz\$6	US-PGPUB; USPAT	OR	ON	2004/07/22 18:10
S6	1	"6304517".PN.	USPAT	OR	OFF	2004/07/22 18:17
S7	28	(tick adj2 counter) and (processor near3 speed)	US-PGPUB; USPAT	OR	ON	2004/07/22 18:21
S8	14	(tick adj2 counter) and (processor near3 speed) and synchroniz\$6	US-PGPUB; USPAT	OR	ON	2004/07/22 19:06
S9	1	("20020143998").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/07/22 19:07
S10	1	("6611922").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/07/23 15:41

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S11	1	("6182182").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/03/05 08:53
S12	1	("6453339").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/03/05 08:54
S13	1	("6769021").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/03/05 09:02
S14	1	("6182182").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/03/05 11:23
S15	1	("6199169").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/03/05 12:06
S16	2	((("6052375") or ("5463620"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/03/07 09:21
S17	1	("6438592").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/03/07 13:27
S18	2	((("6003065") or ("6456388"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/03/07 13:36
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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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IEEE JNL IEEE Journal or Magazine

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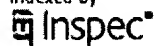
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### 1 [Minimal multitasking operating systems for real-time controllers](#)



Geoffrey H. Kuenning

October 1981

**Proceedings of the 1981 ACM SIGSMALL symposium on Small systems and SIGMOD workshop on Small database systems**

Publisher: ACM Press

 Full text available: pdf(643.54 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In many dedicated microprocessor applications, a full-feature operating system is not required. A methodology is presented for the design of extremely minimal operating systems for such applications. The emphasis is on providing the most basic facilities quickly, without precluding later improvements and additions.

### 2 [Virtual Hardware Prototyping through Timed Hardware-Software Co-Simulation](#)

Franco Fummi, Mirko Loghi, Stefano Martini, Marco Monguzzi, Giovanni Perbellini, Massimo Poncino

March 2005

**Proceedings of the conference on Design, Automation and Test in Europe - Volume 2 DATE '05**

Publisher: IEEE Computer Society

 Full text available: pdf(208.94 KB) Additional Information: [full citation](#), [abstract](#), [index terms](#)

Designers of factory automation applications increasingly demand for tools for rapid prototyping of hardware extensions to existing systems and verification of resulting behaviors through hardware and software co-simulation. This work presents a framework for the timing-accurate co-simulation of HDL models and their verification against hardware and software running on an actual embedded device of which only a minimal knowledge of the current design is required. Experiments on real-life applicat ...

### 3 [MINI-EXEC: a portable executive for 8-bit microcomputers](#)



Thomas L. Wicklund

 November 1982 **Communications of the ACM**, Volume 25 Issue 11

Publisher: ACM Press

 Full text available: pdf(578.22 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

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**Keywords:** microprocessor control systems, multitasking, real-time executives, software portability

4 Let caches decay: reducing leakage energy via exploitation of cache generational behavior



Zhigang Hu, Stefanos Kaxiras, Margaret Martonosi

May 2002 **ACM Transactions on Computer Systems (TOCS)**, Volume 20 Issue 2

**Publisher:** ACM Press

Full text available: pdf(873.03 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

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Elaine Cheong, Jie Liu

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 2 DATE '05**

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Full text available: pdf(178.34 KB)

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6 Formal languages: Towards direct execution of esternel programs on reactive processors



Partha S. Roop, Zoran Salcic, M.W. Sajeewa Dayaratne

September 2004 **Proceedings of the 4th ACM international conference on Embedded software EMSOFT '04**

**Publisher:** ACM Press

Full text available: pdf(269.22 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

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**Keywords:** ARE-Bench Auckland reactive benchmark, direct ESTEREL execution, reactive processor architectures

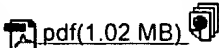


7 Prediction caches for superscalar processors

James E. Bennett, Michael J. Flynn

December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture****Publisher:** IEEE Computer Society

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[Publisher Site](#)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

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8 Workshop on architectural support for security and anti-virus (WASSA): Towards the issues in architectural support for protection of software execution

Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, Mrinmoy Ghosh

March 2005 **ACM SIGARCH Computer Architecture News**, Volume 33 Issue 1**Publisher:** ACM Press

Full text available:



pdf(436.30 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

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9 A Mechanism for Online Diagnosis of Hard Faults in Microprocessors

Fred A. Bower, Daniel J. Sorin, Sule Ozev

November 2005 **Proceedings of the 38th annual IEEE/ACM International Symposium on Microarchitecture MICRO 38****Publisher:** IEEE Computer Society

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[Publisher Site](#)Additional Information: [full citation](#), [abstract](#)


We develop a microprocessor design that tolerates hard faults, including fabrication defects and in-field faults, by leveraging existing microprocessor redundancy. To do this, we must: detect and correct errors, diagnose hard faults at the field deconfigurable unit (FDU) granularity, and deconfigure FDUs with hard faults. In our reliable microprocessor design, we use DIVA dynamic verification to detect and correct errors. Our new scheme for diagnosing hard faults tracks instructions' core struct ...

10 Cache decay: exploiting generational behavior to reduce cache leakage power

Stefanos Kaxiras, Zhigang Hu, Margaret Martonosi

May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture ISCA '01**, Volume 29 Issue 2

**Publisher:** ACM Press

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*This paper examines methods for reducing leakage power within the cache memori ...*


11 Efficient kernel support for reliable communication



Robert D. Russell, Philip J. Hatcher

February 1998 **Proceedings of the 1998 ACM symposium on Applied Computing**

**Publisher:** ACM Press

Full text available:  [pdf\(998.75 KB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

**Keywords:** interprocessor communication, kernel implementation, lightweight protocol, low-cost timeout facilities, shared buffers


12 Configurable flow control mechanisms for fault-tolerant routing



Binh Vien Dao, Jose Duato, Sudhakar Yalamanchili

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture ISCA '95**, Volume 23 Issue 2

**Publisher:** ACM Press

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Fault-tolerant routing protocols in modern interconnection networks rely heavily on the network flow control mechanisms used. Optimistic flow control mechanisms such as wormhole routing (WR) realize very good performance, but are prone to deadlock in the presence of faults. Conservative flow control mechanisms such as pipelined circuit switching (PCS) insures existence of a path to the destination prior to message transmission, but incurs increased overhead. Existing fault-tolerant routing proto ...


13 Time and space profiling for non-strict, higher-order functional languages



Patrick M. Sansom, Simon L. Peyton Jones

January 1995 **Proceedings of the 22nd ACM SIGPLAN-SIGACT symposium on Principles of programming languages**

**Publisher:** ACM Press

Full text available:  [pdf\(1.28 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We present the first profiler for a compiled, non-strict, higher-order, purely functional language capable of measuring time as well as space usage. Our profiler is implemented in a production-quality optimising compiler for Haskell, has low overheads, and can successfully profile large applications. A unique feature of our approach is that we give a formal specification of the attribution of execution costs to cost centres. This specification ena ...


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Because the VPB bus must work properly at power up (and its **timing** cannot be altered if it does not ... **synchronization** when **processor** frequency varies. ...

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resulting in the same execution **timing**. The MAM can truly be turned off by setting the ...

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The MAM can truly be turned off by setting the fetch **timing** value in MAMTIM to one ...

**synchronization** when **processor** frequency varies. ...

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**synchronization** when **processor** frequency varies. Also used during debug mode entry to

enable ... **Clock Tick Counter. Value** from the clock divider. ...

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Assists debugger **synchronization** when **processor** frequency varies. Bi-directional pin

with internal ... **Clock Tick Counter. Value** from the clock divider. ...

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saves power while resulting in the same execution **timing**. The MAM can truly be turned ...

Assists debugger **synchronization** when **processor** frequency varies. ...

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This allows tuning MAM **timing** to match the **processor** operating ... Serial clock

**synchronization** allows devices with different bit rates to communicate via ...

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Serial clock **synchronization** can be used as a handshake mechanism to suspend and resume serial transfer. • Supports **normal** (100kHz) and fast (400kHz) ...  
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